In the Claims

1. (Currently amended) A pixel structure comprising:

a semiconductor substrate;

a radiation sensitive source of carriers in the substrate;

a region in the substrate for collecting but not storing carriers;

at least one doped or inverted region of a first conductivity in or on the substrate; and

at least one planar current flow, carrier transport pathway from or through the region in the substrate for collecting but not storing carriers, to the at least one doped or inverted region, in which carrier transport pathway carriers are not stored ~~during image integration~~ , there being no means for storing carriers in between the region for collecting but not storing carriers and the at least one planar current flow, carrier transport pathway.

2. (Withdrawn) The pixel structure according to claim 1, wherein the non-carrier storing, carrier collecting region has a concentration so low that it is in normal use always depleted.

3. (Withdrawn) The pixel structure according to claim 2, wherein at least part of the non-carrier storing, carrier collecting region is a pinned or buried diode.

4. (Withdrawn) The pixel structure according to claim 1, wherein the non-carrier storing, carrier collecting region is substrate under a covering oxide layer.

5. (Withdrawn) The pixel structure according to claim 1, wherein the non-carrier storing, carrier collecting region is substrate under a field oxide layer.

6. (Previously presented) The pixel structure according to claim 1, wherein the region for collecting but not storing carriers is substrate under a polysilicon cover layer.

7. (Previously presented) The pixel structure according to claim 1, wherein the region for collecting but not storing carriers is diffusion limited.

8. (Previously presented) The pixel structure according to claim 1, further comprising at least one implant confining the region for collecting but not storing carriers along at least one dimension thereof.

9. (Previously presented)The pixel structure according to claim 1, further comprising regions of a second conductivity type in or on the substrate avoiding touching of the region for collecting but not storing carriers and a field oxide.

10. (Original) The pixel structure according to claim 1, wherein the pixel is MOS-based.

11. (Withdrawn) A pixel array comprising at least one set of pixels of a first sensitivity and at least a second set of pixels of a second sensitivity, the first and second sensitivities being different from each other.

12. (Withdrawn) A pixel array comprising a plurality of pixel structures, each pixel structure comprising:

a photosensitive element for converting radiation into charge carriers;

a carrier storing element;

a first switch located in-between said photosensitive element and said carrier storing element; and said photosensitive element also being connected to a voltage with a reset switch; and the pixel array further comprising:

a timing circuit for resetting all the pixels of the array simultaneously.

13. (Withdrawn) A pixel array according to claim 12, wherein the carrier storing element of at least one pixel is an analog memory element such as a capacitor or a parasitic capacitor.

14. (Withdrawn) A pixel array according to claim 12, wherein each pixel is MOS-based.

15. (Withdrawn) A pixel array according to claim 12, further comprising an amplifier connected to each carrier storing element.

16. (Withdrawn) A pixel array according to claim 15, wherein an amplifier is located within at least one pixel structure to have an active pixel.

17. (Withdrawn) A pixel array according to claim 15, wherein an amplifier is placed outside at least one pixel structure to obtain a passive pixel.

18. (Withdrawn) A pixel array comprising a plurality of pixels, each pixel comprising: a photosensitive element for converting radiation into charge carriers;

a carrier storing element;

a first switch located in-between said photosensitive element and said carrier storing element; and said photosensitive element also being connected to a voltage with a reset switch;

and the pixel array further comprising:

a timing circuit for simultaneously opening the first switches of all the pixels of the array simultaneously.

19. (Withdrawn) A pixel array according to claim 18, wherein the carrier storing element of at least one pixel is an analog memory element such as a capacitor or a parasitic capacitor.

20. (Withdrawn) A pixel array according to claim 18, wherein each pixel is MOS-based.

21. (Withdrawn) A pixel array according to claim 18, further comprising an amplifier connected to each carrier storing element.

22. (Withdrawn) A pixel array according to claim 21, wherein an amplifier is located within at least one pixel structure to have an active pixel.

23. (Withdrawn) A pixel array according to claim 21, wherein an amplifier is placed outside at least one pixel structure to obtain a passive pixel.

24. (Withdrawn) A range pixel comprising: a semiconductor substrate;

a radiation sensitive source of carriers in the substrate;

a non-carrier storing, carrier collecting region in the substrate;

at least two doped or inverted regions of a first conductivity type in or on the substrate; and

a non-carrier storing, planar current flow, carrier transport pathway from or through the carrier collecting region to each doped or inverted region.